

AMENDMENTS TO THE SPECIFICATION AND ABSTRACT

In the Specification:

Page 1

Please amend the paragraph beginning on line 8 as follows:

With the progress of information communication devices in recent years, research and development ~~are being made~~has been undertaken for increasing the packing density and capacity of semiconductor devices such ~~DRAM~~DRAMS (Dynamic Random Access Memory). In the circuit layout design of DRAM etc., a necessary electric circuit is placed in an area allocated on a Si (silicon) substrate under certain design rules (dimensional restrictions such as minimum processing dimensions). Each element or component (FET etc.) of the electric circuit is electrically isolated from other elements by use of a structure called "shallow trench isolation" (STI), in which a shallow trench is formed on the Si substrate and the trench is filled with silicon oxide etc. for electrical insulation.

Please amend the paragraph beginning on line 23 and bridging page 2 as follows:

As methods for forming element isolation parts (fields) and ~~actives~~active ~~areas~~, a method forming trenches and filling them with insulating material, a method forming thermally-oxidized films, etc. have been disclosed in JP-A-1-223741, JP-A-4-42948, JP-A-8-241922, JP-A-8-279553, etc.

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Please amend the paragraph beginning on line 8 as follows:

In DRAM whose storage capacity is increasing constantly, the miniaturization and high integration are being promoted in its sense amplifier circuit as well as in its memory section. In conventional circuit layout designing methods, the miniaturization of the sense amplifier circuit is basically carried out by simply scaling down the circuit layout of previous-generation sense amplifier circuit having larger processing dimensions, therefore, the difference in the STI trench width tended to be maintained. Meanwhile, by the micromachining technology of recent years, the STI trench width has become as narrow as approximately $0.2 \mu m$ at its narrowest part.

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Please amend the paragraph beginning on line 28 and bridging page 30 as follows:

Fig. 2 shows the cross-sectional structure of the semiconductor device of this embodiment (cross sections taken along lines A to [[G]]E in Fig. 1). An n-channel FET 10 is composed of n-type sources/drains 12 and 13 which are formed in a p-type well 11 of the Si substrate 1, a gate insulation layer 14, a gate 15 (G1, G2), and silicide layers 17 and 18 formed on the top surfaces of the gate 15 and the sources/drains 12 and 13. A p-channel FET 30 is composed of p-type sources/drains 32 and 33 which are formed in an n-type well 31 (N-WELL) of the Si substrate 1, a gate insulation layer 34, a gate 35 (G3, G4), and silicide layers 37 and 38 formed on the top surfaces of the gate 35 and the sources/drains 32 and 33. Each transistor is insulated from other elements by the shallow trench isolation 2 containing material (SiO_2 , SiN , etc.) having resistance higher than that of the